

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2024	(Semester)	2	(Course No.)	2150084301
(Class)	01	(Open to)	3, 4	(Course Classification)	-IT / -
/	3.0 / 03 / 3		100	가	가
(Office)	10704	(Telephone)	02-828-7489	(e-mail)	inchul.song@ssu.ac.kr
	(FL), (PBL)		+		2023
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
	(C),				
(Course Description)	, CAD tool , HDL(Hardware Description Language)				

Verilog HDL	

가	(100)	(100%)
	100	100

(Required Texts)		* /Digital System Designs and Practices////Ming-Bo Lin/Wiley/2008/
		* /Modeling, synthesis, and rapid prototyping with the Verilog HDL/M Ciletti/Prentice-Hall/1999/
	()	* /HDL SOC IP / / /2004/
		* //2023
	:	(C)
	- Engaged learning .	
	- . ,	
	- : 50%, 15%, 25%, 10%	

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2.

(Week)	(Keyword)	(Description)		(Texts)
01		HDL		,
02	Verilog HDL	Verilog HDL syntax.		,
03	Dataflow			, ()
04	Simulation	Verilog HDL S/W , simulation , Testbench	, , ,	,
05	Behavioral	Behavioral H/W	,	,
06	Behavioral	Behavioral ,	,	,
07	Behavioral	Behavioral .	,	,
08		: microprocessor/FIR filter .	, ,	,
09	FSM	Finite state machine - state diagram, :	, , , , ,	,
10	FSM	Finite state machine - ASM chart, :	, , , , ,	,
11	, task,	Verilog HDL system task . :	, ,	,
12		(/)		/
13	RTL(Register Transfer Level)	RTL(Register Transistor Level) , :	, ,	,
14	Design example	Design example: Combinational logic, :	, ,	,
15	Design example	Design example: sequential logic,	, ,	,

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3. ()

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	Open-ended problem		
	Teamwork		
	Communication skills		